Midterm Exam

(February 20th @ 7:30 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (20 pts)

- Compute the result of the following operations. The operands are signed fixed-point numbers. The result must be a signed fixed-point number. For the division, use $x = 5$ fractional bits.

1.0111 + 1.101001	1.010101 − 1000.0101	01.11111 + 0.10001
10.101 × 1.01101	1.001 × 0.1011	10.1010 ÷ 0.101

Problem 2 (10 pts)

- Represent these numbers in Fixed Point Arithmetic (signed numbers). Select the minimum number of bits in each case.
  - ✓ -32.125
  - ✓ 17.75

- Complete the table for the following fixed point formats (signed numbers): (6 pts.)

Integer bits	Fractional Bits	FX Format	Range	Resolution
8	6			
6	4			

Problem 3 (40 pts)

- Calculate the result (provide the 32-bit result) of the following operations with 32-bit floating point numbers. Truncate the results when required. When doing fixed-point division, use 4 fractional bits. Show your procedure.

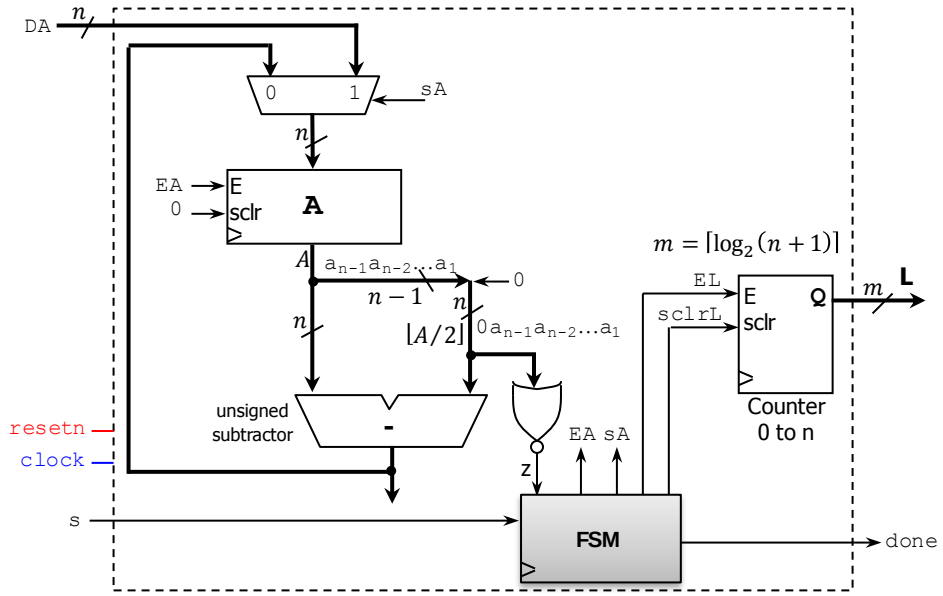
✓ 40D00000 + C2EA0000	✓ 50A90000 − 4F480000	✓ 80200000 × 7AB80000	✓ FB380000 ÷ 48C00000

Problem 4 (30 pts)

- "Integer Base-2 Logarithm": This circuit computes $L = \lceil \log_2 A \rceil$, where A is an unsigned n-bit number stored in register A. The digital system is depicted below: FSM + Datapath. Example: For $n = 8$: if $A = 00110110$, then $L = 0110$.
  - ✓ Note that for $n = 8$, if $A = a_7a_6a_5a_4a_3a_2a_1a_0$, then $\lfloor A/2 \rfloor = 0a_7a_6a_5a_4a_3a_2a_1$. Also: $z = 1$ if $\lfloor A/2 \rfloor = 0$.
  - ✓ m-bit counter: $sclr$. If $E = sclr = 1$, the count is initialized to zero. If $E = 1, sclr = 0$, the count is increased by 1.
  - ✓ Register: If $E = 1$: $sclr = 1 \rightarrow$ Clear, $sclr = 0 \rightarrow$ Load.

- Sketch the Finite State Machine diagram (in ASM form) given the algorithm (for $n = 8$, $m = 4$). (18 pts.)
  - ✓ The process begins when s is asserted, at this moment we capture DA on register A. Then the process continues by updating A and it is concluded when $A = 1$. The signal $done$ is asserted when we finish computing $\lceil \log_2 A \rceil$.

- Complete the timing diagram where $n = 8, m = 4$. (12 pts.)



ALGORITHM

```
L ← 0
while A ≠ 1
    A ← A - ⌊A/2⌋
    L ← L + 1
end while
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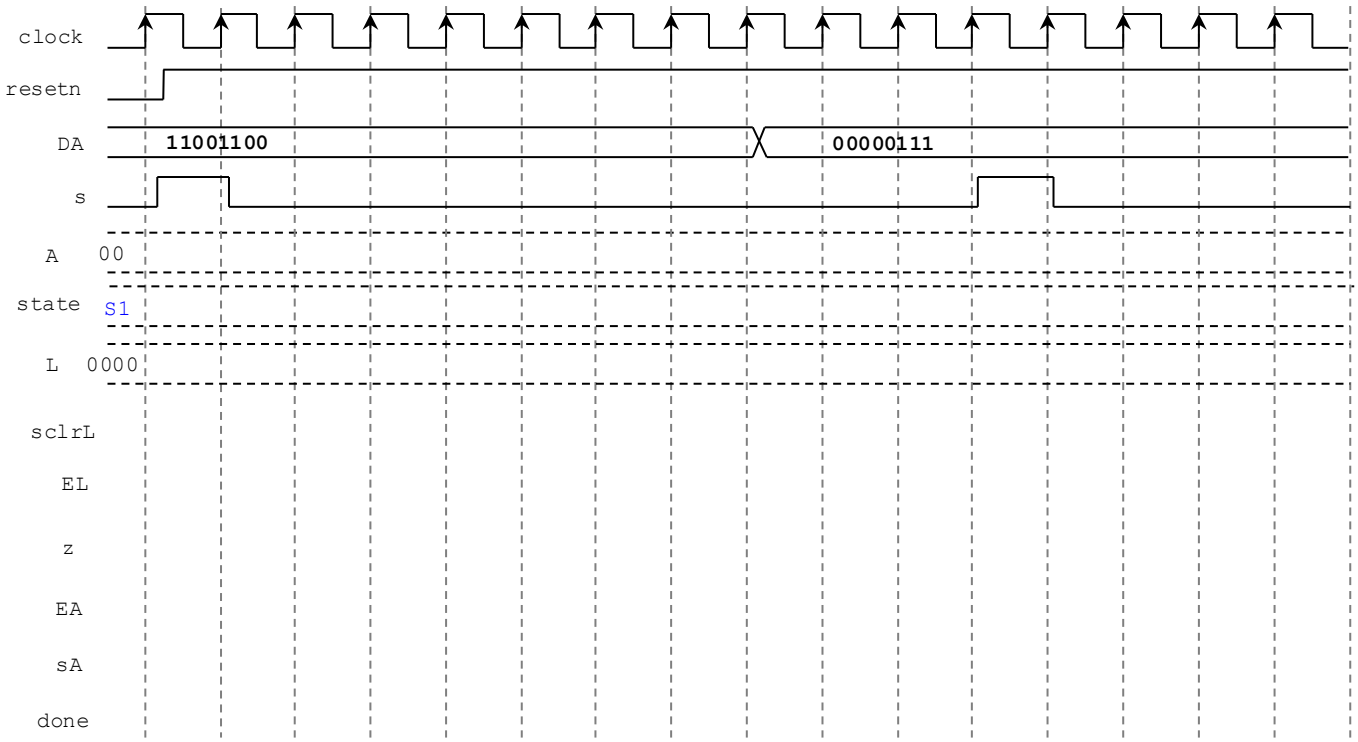
clock
resetn
DA
11001100
00000111
s
A
00
state
S1
L
0000
sclrL
EL
z
EA
sA
done